REMARKS

Claims 2-4 are pending in the application. Claims 1-3 were rejected under 35 U.S.C. § 103 (a), as described in paragraph 3 of the Office Action. Claim 4 is the only independent claim.

The specification has been amended to place the application in correct idiomatic English.

Claims 2 and 3 have been amended to be dependent upon newly added independent claim 4, and to avoid being construed under 35 U.S.C. § 112, sixth paragraph.

It is respectfully submitted that the outstanding rejection of claim 1 is moot, as the claim has been cancelled. Cancellation of claim 1 is not an acquiescence that the claim is not patentable over the prior art of record.

As suggested in paragraph 1 of the Office Action, attached hereto are replacement formal drawings for Figs. 7-9, wherein each of Fig. 7-9 have been designated by a legend - -Prior Art- -.

Applicants filed an Information Disclosure Statement (IDS) on March 6, 2001 and an IDS on June 6, 2001. Each of the March 6th and June 6th IDS's included a Form PTO-1449 listing the references cited therein, respectively. Each of the March 6th and June 6th IDS's were filed in compliance with 37 CFR § 1.97 and 1.98. Therefore, the references cited in the March 6th and June 6th IDS's should have been considered. However, the Office Action fails to include initialed copies of the Forms PTO-1449 corresponding to the March 6th and June 6th IDS's.

In light of the above discussion, Applicants respectfully request initialed copies of the Forms PTO-1449 corresponding to the March 6th and June 6th IDS's, clearly indicating that the references cited therein have been considered by the Office.

Applicants submit that claims 2-4 are patentable over the prior art of record for the following reasons.

The invention in accordance with the present invention, for example as illustrated in Fig. 1, is drawn to a digital signal processor comprising a main arithmetic device 11 and auxiliary arithmetic device 12. The auxiliary arithmetic device 12 includes a reservation processing register 26 and a clear circuit 27. The auxiliary arithmetic device 12 is operable to execute a task corresponding to a task demand received from the main arithmetic device 11, which has been set in the reservation processing register 26, after terminating a processing task.

In accordance with one aspect of the present invention, the auxiliary arithmetic device 12 receives a task demand from the main arithmetic device 11, even though the auxiliary arithmetic device 12 is currently processing a series of tasks. The auxiliary arithmetic device 12 is operable to set the task demand in the reservation processing register 26 and execute an interrupt task corresponding to the task demand, only once, and then clear circuit 27 clears the task demand from the reservation processing register 26.

Accordingly, in accordance with the present invention, for example as illustrated in Figs. 2, 4 and 6, when the auxiliary arithmetic device 12 receives a task demand from the main arithmetic device 11 while it is processing a task, the auxiliary arithmetic device 12 can execute the demanded task only once during a one-cycle processing period.

The above discussed feature is recited in claim 4, as discussed below.

The digital signal processor of claim 4 recites a main arithmetic device operable to generate a task demand and an auxiliary arithmetic device operable to receive the task demand from the main arithmetic device and to perform the task. The auxiliary arithmetic device of claim 4 comprises a program memory area having a task list stored therein, a reservation processing register and a clear circuit. The clear circuit of claim 4 is operable "**to clear the task demand in said reservation processing register after the interrupt task corresponding to the task demand set in said reservation processing register is executed.**" Further, claim 4 recites that "said auxiliary arithmetic device is operable to execute the interrupt task corresponding to the task demand from said main arithmetic device **only once**, after terminating processing of one of the plurality of tasks which are defined in said task list."

Applicants admitted prior art (APA) and Carmon, either singly or in combination, fails to disclose or suggest the above identified limitations.

As discussed in page 3 of the Office Action, the APA does not teach an auxiliary device providing a reservation processing register and a clear circuit. Therefore, the APA fails to teach an auxiliary arithmetic device, as recited in independent claim 4.

Carmon fails to disclose or suggest the shortcomings of the APA, such that a combination of the disclosures of the APA and Carmon would disclose or suggest that which is recited in independent claim 4.

Carmon discloses an operating system for executing task demands from a host processor, comprising a task execution priority queue (list) and idle list. The task execution priority queue includes a list of tasks, wherein the tasks are listed in accordance with their respective completion deadlines. The idle list includes tasks that have already been executed and are awaiting their next restart times. Tasks of the idle list are arranged corresponding to various levels of interrupt sources. As disclosed in column 13, lines 40-55 of Carmon, when an interrupt occurs while tasks are being executed in accordance with the task execution priority queue, the idle list associated with the interrupt level is checked, and tasks of the processing start time associated to the interrupt level are removed from the idle list. As discussed in column 13, lines 56-65 of Carmon, it is then judged whether the priority of the tasks to be removed is higher than the priority of a task that is presently executed, and accordingly the status of the task that is presently being executed is saved or the task that is presently being executed is allowed to resume.

Carmon does not disclose or suggest executing an interrupt task corresponding to a task demand from the main arithmetic device only once and then clearing the task as in the processor of the present invention. On the contrary, Carmon discloses that when an interrupt occurs, tasks in the idle list are cleared. However, these tasks in the idle list have already been executed and are awaiting their next restart times. Accordingly, the system of Carmon cannot execute the task demanded from the main arithmetic device **only once** and then clear the task as in the processor of the present application.

In light of the above discussion, it is apparent that Carmon fails to disclose or suggest: a clear circuit that is operable to clear the task demand in the reservation processing register after the interrupt task corresponding to the task demand set in the reservation processing register is executed or an auxiliary arithmetic device that is operable to execute the interrupt task corresponding to the task demand from the main arithmetic device only once, after terminating processing of one of the plurality of tasks, as recited in independent claim 4.

Because neither the APA nor Carmon discloses or suggests the clear circuit or the auxiliary arithmetic device, as recited in independent claim 4, a combination of the disclosures of the APA and Carmon would additionally fail to disclose or suggest that which is recited in independent claim 4.

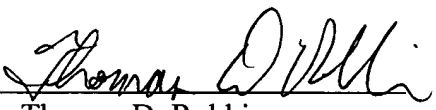
Furthermore, because of the differences between independent claim 4 and the cited prior art, as discussed above, one of ordinary skill in the art at the time of the invention would not have been motivated to modify the teachings of the applied prior art to arrive at that which is recited in independent claim 4. Accordingly, claim 4, and dependent claims 2 and 3, are patentable over the prior art of record.

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

Yasushi IMAMURA et al.

By: 

Thomas D. Robbins
Registration No. 43,369
Attorney for Applicants

TDR/jlg
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
October 12, 2004